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APPLICATION N	0.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/667,709 09/22/2000		09/22/2000	Philip William Gillis	2925-0431P 9953	
30594	7590	01/28/2004	EXAMINER CHANG, SUNRAY		
	-	CKEY & PIERCE,			
P.O. BOX RESTON,		20195	ART UNIT	PAPER NUMBER	
				2128	4
				DATE MAILED: 01/28/2004	,

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(a)					
,	Application No.	Applicant(s)					
	09/667,709	GILLIS, PHILIP WILLIAM					
Office Action Summary	Examiner	Art Unit					
	Sunray Chang	2128					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).							
1)⊠ Responsive to communication(s) filed on 22 Se	entember 2000						
,							
 2a) This action is FINAL. 2b) This action is non-final. 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. 							
Disposition of Claims							
4) Claim(s) 1-30 is/are pending in the application.							
4a) Of the above claim(s) is/are withdrawn from consideration.							
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>1 - 30</u> is/are rejected.							
7) Claim(s) is/are objected to.							
8) Claim(s) are subject to restriction and/o	r election requirement.						
Application Papers							
9)☐ The specification is objected to by the Examine	r.						
10)⊠ The drawing(s) filed on is/are: a)⊠ acc	epted or b) \square objected to by the $\mathfrak l$	Examiner.					
Applicant may not request that any objection to the	drawing(s) be held in abeyance. See	e 37 CFR 1.85(a).					
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).							
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority under 35 U.S.C. §§ 119 and 120							
12)							
Attachment(s)	,, , , , , , , , , , , , , ,						
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) 		(PTO-413) Paper No(s) atent Application (PTO-152)					
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2		atom representation (i 10-102)					

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DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 1. Claims 1 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Jean-Louis Lassorie (U.S. Patent No. 5,515,382 and Lassorie hereinafter).
- 2. Regarding Independent claim 1, Lassorie teaches receiving (received, Col 3, Line 12) a message (configuration parameter, Col 3, Line 12) from a system (shift register, Col 3, Line 13); comparing (compared, Col 12, Line 55) the received message (results, Col 12, Line 54) to information (reference value, Col 12, Line 55) stored (storing, Col 11, Line 37) in a response file (characteristic data, Col 11, Line 38) used to simulate system response (simulation, Col 12, Line 56), the response file (characteristic data, Col 11, Line 38) including at least one message (number, Col 11, Line 38), a message marker associated with each message (control signals, Col 11, Line 39), at least one response (length of the data words, Col 11, Line 40) associated with each message, and an end-of-response marker (access time, Col 11, Line 40) associated

with each response; and simulating a response (simulation, Col 12, Line 56) to the system message (reference value, Col 12, Line 55) by outputting a response (result, Col 12, Line 54) stored in association with a stored message (characteristic data, Col 11, Line 38) matching the received message (reference data, Col 10, Line 55), upon the received message (data resulting, Col 10, Line 53) matching a message stored in the response file (characteristic data, Col 11, Line 38), wherein upon at least two responses (number and nature, Col 11, Line 38) being stored in association with a message (memory, Col 11, Line 41), the at least two responses (number and nature, Col 11, Line 38) are sequentially output (serial data output, Col 6, Line 61) in response to sequential receipt (serial data input, Col 6, Line 59) of the message.

- 3. Regarding dependent claims 2, 12 and 22, Lassorie teaches simulation process (executing the test program, Col 12, Line 39) occurs within the system (internal data memory, Col 12, Line 47).
- 4. Regarding dependent claims 3, 13 and 23, Lassorie teaches simulation process (executing the test program, Col 12, Line 39) occurs within a device (integrated circuit, Col 12, Line 40) separate from, but operatively (executing, Col 12, Line 39) connected (step, Col 12, Line 39) to the system (test program, Col 12, Line 39).
- 5. Regarding dependent claims 4, 14 and 24, Lassorie teaches the response file (characteristic data, Col 11, Line 38) includes at least one autonomous response

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(access time, Col 11, Line 40), wherein the autonomous response is output a predetermined time (one clock period, Col 10, Line 38) after simulation begins, irrespective (no complete, Col 10, Line 40) of a received message (instruction, Col 10, Line 401).

- 6. Regarding dependent claims 5, 15 and 25, Lassorie teaches the response file (characteristic data, Col 11, Line 38) includes at least one autonomous response (access time, Col 11, Line 40), wherein the autonomous response is periodically output (one clock period, Col 10, Line 38) irrespective (no complete, Col 10, Line 40) of a received message (instruction, Col 10, Line 401).
- 7. Regarding dependent claims 6, 16 and 26, Lassorie teaches the response file (characteristic data, Col 11, Line 38) includes at least two different messages (number and nature, Col 11, Line 38), each associated with at least one response (characteristic data, Col 11, Line 38).
- 8. Regarding dependent claims 7, 17 and 27, Lassorie teaches storing (stored, Col 9, Line 30) a record (procedure, Col 9, Line 28) of a received message (application of the circuit, Col 9, Line 29), wherein upon a message (data input, Col 9, Line 13) being received a second time (serial entry the other values, Col 9, Line 12), either a second response (other value, Col 9, Line 12) stored in association with the received message (serial entry, Col 9, Line 12) is output, or the first response (last elementary cell, Col 6,

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Line 42) is again output if no second response is stored in association with the received message (data output, Col 6, Line 45).

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- 9. Regarding dependent claims 8, 9, 18, 19, 28 and 29, Lassorie teaches sequential responses (serial input, Col 6, Line 42) stored in the response file (shift register, Col 6, Line 38) in association with a common message (data, Col 6, Line 38) are sequentially output (serial output, Col 6, Line 43) upon successive receipt (input, Col 6, Line 41) of the common message.
- 10. Regarding dependent claims 10, 20 and 30, Lassorie teaches the response file (shift register, Col 6, Line 38) is created using a log file (interface device, Col 12, Line 27) of the system.
- 11. Regarding independent claims 11 and 21, Lassorie teaches a memory (shift register, Col 11, Line 36), adapted to store (storing, Col 11, Line 37) a response file (reference data, Col 10, Line 55), the response file being used to simulate (testing, Col 11, Line 34) system (circuit, Col 11, Line 35) response (makeup, Col 11, Line 35) and including at least one message (number, Col 11, Line 38), a message marker (control signal, Col 11, Line 39) associated with each message (Col 11, Line 38 42), at least one response (length of the data words, Col 11, Line 40) associated with each message, and an end-of-response marker (access time, Col 11, Line 40) associated with each response; a comparator (comparator, Col 10, Line 6), adapted to compare a

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message (data resulting, Col 10, Line 53) received from a system (execution of the program, Col 10, Line 54) to information (reference data, Col 10, Line 55) stored in the response file (register, Col 10, Line 55) to determine (detected, Col 10, Line 57) whether or not the received message (data resulting, Col 10, Line 53) matches a message (reference data, Col 10, Line 55) stored in the response file; and an output device (comparator, Col 10, Line 6) adapted to simulate a response (execution of the program, Col 10, Line 54) to the system message (reference data, Col 10, Line 55), upon determining (detected, Col 10, Line 57) that a received message (data resulting, Col 10, Line 53) matches a message (reference data, Col 10, Line 55) stored in the response file, by outputting (read through, Col 10, Line 54) a response (data resulting, Col 10, Line 53) stored in association with the matching stored message (reference data, Col 10, Line 55), wherein upon at least two responses (number and nature, Col 11, Line 38) being stored in association with a message (memory, Col 11, Line 41), the at least two responses are sequentially output (serial data output, Col 6, Line 61) in response to sequential receipt (serial data input, Col 6, Line 59) of the message.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gallo et al. (U.S. Patent No. 5,563,959) discloses predetermined, serial string, storage and comparison. Hasebe et al. (U.S. Patent No. 5,613,062) discloses logic simulation, sequentially, storage, time period, predetermined. Van Brunt (U.S. Patent No. 4,527,249) discloses comparator as an input, sequence. Shoji et al.

(U.S. Patent No. 5,475,832) discloses serial, predetermined simulation time, storing,

memory.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sunray Chang whose telephone number is 703-305-8744. The examiner can normally be reached on M-F 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703-305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-746-3506.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-6833.

Sunray Chang Patent Examiner Group Art Unit 2128 Technology Center 2100 U.S. Patent and Trademark Office

January 9, 2004

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